

Customer No.: 31561
Application No.: 10707,666
Docket No.: 12057-US-PA

In The Claims:

Claim 1. (Currently amended) A dual slope analog-to-digital converter, comprising:

an input circuit;

an integrator;

a comparator;

an offset cancellation logic;

a hysteresis logic;

a control logic; and

a data counter,

wherein the input circuit selectively supplies a plurality of input voltages and a plurality of reference voltages to the integrator, the control logic determines a first reference voltage for providing for the input circuit during initialization, being integrated by the integrator, a residual voltage is determined as a second reference voltage is provided during discharge period, the data counter converts an input voltage to a digital data corresponding to the discharge period, the offset cancellation logic determines an offset value from the first reference voltage during an offset cancellation cycle and compares which with input value that is to be converted, and the hysteresis logic updates the output value comparing a newly converted value during the current measurement cycle and a previous value converted in a previous measurement cycle ~~[determines output value]~~.

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Claim 2-6. (Cancelled)

Claim 7. (Currently amended) The dual slope analog-to-digital converter as recited in claim 1, wherein the hysteresis logic comprises:

at least a first data register, for storing the first input ~~[reference]~~ voltage in digital form; and

a ~~[second]~~ subtractor, the subtractor calculates the difference between a newly converted value during the current measurement cycle and the previous value converted in the previous measurement cycle and stored in the data register, the hysteresis logic updates the data register with the newly converted value if the difference is bigger than a predetermined value~~[for operating on a value provided by the first subtractor and first data register, and save resulting value to the first data register]~~.

Claim 8. (Cancelled)

Claim 9. (Currently Amended) The dual slope analog-to-digital converter as recited in claim 1, where[-]in the control logic determines input signal to the first operational amplifier to be the first reference voltage, the second reference voltage, and at least one of a first input voltages, and at least controls a switch between the input amplifier and the integrator, the control logic comprises:

a first inverter, for inverting output signal of the comparator; and

a second inverter, coupling across the switch, for inverting output signal of the first

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inverter_[7]

Claim 10. (Original) A dual slope analog-to-digital converting method, comprising a plurality of cycles, each one of the cycles comprises an integrating period, a discharge period, the dual slope analog-to-digital converting method comprises:

- performing an initialization cycle;
- performing an offset cancellation cycle;
- performing a first measurement cycle, for providing a first channel for converting a first input voltage, wherein the initialization cycle, the offset cancellation cycle, and the first measurement cycle are performed in a sequence as cited;
- providing a first reference voltage during the integrating period of the initialization cycle, providing a second reference voltage during the discharge period of the initialization cycle for generating a residual voltage;
- converting the first reference voltage into digital form and saving which in a constant register during the offset cancellation cycle;
- operating with the first subtractor on the first reference voltage in digital form and the value stored in the constant data register to obtain difference to be saved in an offset register;
- providing the first input voltage during the integrating period of the first measurement cycle, providing a second reference voltage during the discharge period of the first measurement period, converting the first input voltage into digital form and saving which to

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the data counter during the first measurement cycle, and from which subtracting the value saved in the offset register to obtain a new first channel value; and

comparing the new first channel value with the first channel value saved in a data register, if differing larger than a first minimum, the new first channel value takes place in the first data register, and output of the first channel is updated.

Claim 11. (Original) The dual slope analog-to-digital converting method as recited in claim 10, wherein the first input voltage, the first reference voltage are higher than an analog ground voltage level, and the second reference voltage is lower than the analog ground voltage level.

Claim 12. (Original) The dual slope analog-to-digital converting method as recited in claim 11, wherein a dummy cycle is inserted before each the first measurement cycle, and providing the first reference voltage during the integrating period, providing the second reference voltage during the discharge period.

Claim 13. (Original) A dual slope analog-to-digital converting method, comprising a plurality of cycles, each one of the cycles comprises an integrating period, a discharge period, the dual slope analog-to-digital converting method comprises:

performing an initialization cycle;

performing an offset cancellation cycle;

performing a first measurement cycle, for providing a first channel for converting a

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first input voltage,

providing a first reference voltage during the integrating period of the initialization cycle, providing a second reference voltage during the discharge period of the initialization cycle for generating a residual voltage;

converting the first reference voltage into digital form and saving which in a constant register during the offset cancellation cycle;

operating with the first subtractor on the first reference voltage in digital form and the first reference value in digital form stored in the constant register to obtain difference to be saved in an offset register;

providing the first input voltage during the integration period of the first measurement cycle, providing the second reference voltage during the discharge period of the first measurement cycle, converting the first input voltage into digital form and saving which to the data counter during the first measurement cycle, and from which subtracting the value saved in the offset register to obtain a new first channel value;

comparing the new first channel value with the first channel value saved in a first data register, if differing larger than a first minimum, the new first channel value takes place in the first data register, and output of the first channel is updated;

providing the second input voltage during the integrating period of the second measurement cycle, providing the second reference voltage during the discharge period of the

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second measurement cycle, converting the second input voltage into digital form and saving which to the data counter during the second measurement cycle, and from which subtracting the value saved in the offset register to obtain a new second channel value; and

comparing the new second channel value with the second channel value saved in a second data register, if differing larger than the first minimum, the new second channel value takes place in the second data register, and output of the second channel is updated.

Claim 14. (Original) The dual slope analog-to-digital converting method as recited in claim 13, wherein the first input voltage, the first reference voltage are higher than a ground voltage level, and the second reference voltage is lower than the ground voltage level.

Claim 15. (Original) The dual slope analog-to-digital converting method as recited in claim 14 wherein a dummy cycle is inserted before the first measurement cycle and the second measurement value, the dummy cycle comprises providing the first reference voltage during the integrating period, and providing the second reference voltage during the discharge period.